REMARKS

Claims 1-5 and 11-15 stand rejected under 35 USC 102(e) over Ruszczyk (U.S. Pat. 6,205,150). Claims 1 and 2 have been cancelled. Claim 3 has been amended to include the limitations of cancelled Claims 1 and 2.

In Ruszczyk, a "first network device 20 schedules the lower priority data packets in the third queue with transmission deadlines" and "when a transmission deadline for a low priority data packet in the third queue has expired, first network device 20 promotes the low priority data packet to the second queue at step 40 thereby preventing the starvation of transmission time for lower priority data packets." Col. 4, lines 61-63, line 66 to col. 5, line 4; col. 5, lines 40, 56-60; col. 6, lines 15-22; block 40 in Fig. 2; block 54 in Fig. 3.

Ruszczyk does not disclose or suggest a bus between a host processor and a peripheral device configured to receive data during time periods of a predetermined length, as claimed in amended Claim 3 of the present application. Also, Ruszczyk does not disclose or suggest a control circuit configured to (a) place at least a minimum amount of data from a first queue onto the bus during each time period and (b) place data from a second queue onto the bus only when the bus is otherwise unoccupied, as claimed in amended Claim 3 of the present application. The sections of Ruszczyk cited in the Office Action do not disclose or suggest these aspects of amended Claim 3. Applicant respectfully submits that amended Claim 3 is allowable over Ruszczyk.

Claims 4 and 5 have been amended to depend from amended Claim 3 and contain all of the limitations of amended Claim 3.

Applicant respectfully submits that amended Claims 4 and 5 are allowable over Ruszczyk.

Claims 11-12 have been cancelled. Claim 13 has been amended to include all of the limitations of cancelled Claims 11 and 12.

Ruszczyk does not disclose or suggest "placing data on the bus during time periods of predetermined length, where placing data of the first class on the bus includes placing at least a minimum amount of data of the first class onto the bus during each time period; and placing data of the second class onto the bus only when the bus is otherwise unoccupied," as claimed in amended Claim 13 of the present application. Claims 14 and 15 have been amended to depend from amended Claim 13 and contain all of the limitations of amended Claim 13. Applicant respectfully submits that amended Claims 13-15 are allowable over Ruszczyk.

Claims 6 stands rejected under 35 USC 103(a) over Ruszczyk. Claim 6 has been amended to include the limitations of cancelled Claim 1. Claim 6 recites a "Universal Serial Bus" and "isochronous and bulk transfers." The Office Action cites col. 5, lines 61-67 and col. 6, lines 1-26 in Ruszczyk. But these lines do not disclose or suggest a Universal Serial Bus or isochronous and bulk transfers. In contrast, col. 6, lines 15-22 of Ruszczyk state:

> "Once a transmission deadline of a lower priority data packet in a low priority queue 66 has expired, a promoter 70 promotes the lower priority data packet to a high priority queue 62 whereby the promoted data packet is scheduled by guaranteed scheduling method 64. The lower priority data packet will then be sent to the transmitter

72 for execution in the order determined by the guaranteed scheduler 64."

"Round robin scheduling of the queues" is not an example of "isochronous transfers" because "isochronous transfers" are higher priority transfers. "Guaranteed scheduling" is not an example of "bulk transfers" because bulk transfers are lower priority transfers. The present application states "bulk transfers" are used with "lower priority data" "for which only a guarantee of delivery is required. Bulk transfers do not guarantee bandwidth or priority on the bus." Page 1, line 23 to page 2, line 3. Thus, Ruszczyk does not disclose or teach amended Claim 6. Nor does Thomas (U.S. Pat. 5,941,952) disclose or teach amended Claim 6. Applicant respectfully requests that amended Claim 6 be allowed.

Claims 7-10 and 16-19 stand rejected under 35 USC 103(a) over Ruszczyk and "RFC 2212 entitled 'Specification of Guaranteed Quality Service' by Shenker et al." The latter reference was not included in the Office Action sent to the Applicant and was not cited in the Notice of References Cited PTO-892 form. Therefore, the Patent Office has not meet its burden of proving a prima facie case of obviousness under 35 USC 103(a).

Claims 7-10 have been amended to depend from amended Claim 3 and include all of the limitations of amended Claim 3. Applicant respectfully submits that amended Claims 7-10 are allowable over Ruszczyk and Thomas for the reasons stated above.

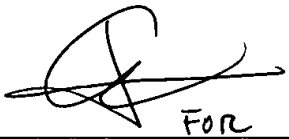
Claims 16-19 have been amended to depend from amended Claim 13 and include all of the limitations of amended Claim 13. Applicant respectfully submits that amended Claims 16-19 are allowable over Ruszczyk and Thomas for the reasons stated above.

New Claims 20-24 have been added. No new matter was added. Applicant respectfully submits that Claims 20-24 are allowable over Ruszczyk and Thomas for the reasons stated above.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be allowed. Enclosed is a Enter $ amount check for excess claim fees. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,



ALEX CHEN
REG NO 45,591

For

Date: 1/9/08

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Version with markings to show changes made

In the claims:

Claims 1, 2, 11 and 12 have been cancelled.

Claims 3-10 and 13-19 have been amended as follows:

3. (Amended) A computer system comprising:

a host processor;

a peripheral device configured to transfer data to the host processor over an attachment bus using at least first and second types of data transfers, comprising:

a classifying circuit configured to separate the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer;

a first queue connected to receive the first class of data from the classifying circuit;

a second queue connected to receive the second class of data from the classifying circuit; and

a control circuit configured to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is configured to receive data during time periods of predetermined length; where the control circuit is configured to place at least a minimum amount of data from the first queue onto the bus during each time period;

[The system of claim 1,] where the control circuit [controller] is configured to place data from the second queue onto the bus only when the bus is otherwise unoccupied.

4. (Amended) The system of claim 3[1], where the peripheral device includes a network interface component connected to receive the data from a computer network.

5. (Amended) The system of claim 3[4], wherein the data includes packetized voice data.

6. (Amended) A computer system comprising:

a host processor;

a peripheral device configured to transfer data to the host processor over an attachment bus using at least first and second types of data transfers, comprising:

a classifying circuit configured to separate the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer;

a first queue connected to receive the first class of data from the classifying circuit;

a second queue connected to receive the second class of data from the classifying circuit; and

a control circuit configured to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

[The system of claim 3[1],] where the bus is a Universal Serial Bus (USB) and the peripheral device is configured to transfer data over the bus using isochronous and bulk transfers.

7. (Amended) The system of claim 3[1], where the peripheral device is configured to deliver the data in packets of predetermined length.

8. (Amended) The system of claim 7, where the classifying circuit is configured to place each of the packets into one of the queues[classes].

9. (Amended) The system of claim 7, where a portion of each packet indicates a channel[the type of transfer] associated with the packet, and where the classifying circuit includes a storage device that stores information indicating each of the channels[types of transfer] that is associated with at least one of the classes.

10. (Amended) The system of claim 9, where the classifying circuit includes a selection element configured to compare, for each packet, the information in the storage device to the data in the portion of the packet that indicates the channel[type of transfer] and configured to select a corresponding one of the queues to receive the packet.

13. (Amended) A method comprising:

transferring data to a host processor over an attachment bus using at least first and second types of data transfers and, in transferring the data:

separating the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer; and

placing data of the first class onto the bus at a higher priority than data of the second class is placed onto the bus.

placing data on the bus during time periods of predetermined length, where placing data of the first class on the bus includes placing at least a minimum amount of data of the first class onto the bus during each time period; and

[The method of claim 11, further comprising] placing data of the second class onto the bus only when the bus is otherwise unoccupied.

14. (Amended) The method of claim 13[11], further comprising receiving the data from a computer network.

15. (Amended) The method of claim 13[14], where receiving the data includes receiving packetized voice data.

16. (Amended) The method of claim 13[11], where transferring data includes delivering the data in packets of predetermined length.

17. (Amended) The method of claim 11[16], where separating the data includes placing each of the packets into one of the queues[classes].

18. (Amended) The method of claim 11[16], further comprising storing information indicating each channel[of the types of transfer] that is associated with at least one of the classes.

19. (Amended) The method of claim 18, further comprising:

comparing, for each packet, the stored information to a portion of the data in the packet that indicates the channel [type of transfer] associated with the packet; and

placing the packet into a corresponding one of the queues [classes].

Please add the following new claims:

20. (New) The system of claim 9, where the classifying circuit comprises a buffer, a shift register and a content addressable memory (CAM) device.

21. (New) The system of claim 3, wherein the bus is a Peripheral Component Interface (PCI) bus.

22. (New) The system of claim 3, wherein the bus uses an Asynchronous Transfer Mode (ATM).

23. (New) A peripheral device coupled between a host device and a network, the peripheral device operable to transfer data packets to the host processor over a bus, the peripheral device comprising:

a classifying circuit operable to identify a priority level of each data packet from the network;

a first queue operable to store data packets with a first priority level from the classifying circuit;

a second queue operable to store data packets with a second priority level from the classifying circuit; and

a control circuit coupled to first and second queues, the control circuit being operable to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is configured to receive data during time periods of predetermined length; the control circuit being configured to place at least a minimum amount of data from the first queue onto the bus during each time period; the control circuit being configured to place data from the second queue onto the bus only when the bus is otherwise unoccupied.

24. (New) A peripheral device coupled between a host device and a network, the peripheral device operable to transfer data packets to the host processor over a bus, the peripheral device comprising:

a classifying circuit operable to identify a priority level of each data packet from the network;

a first queue operable to store data packets with a first priority level from the classifying circuit;

a second queue operable to store data packets with a second priority level from the classifying circuit; and

a control circuit coupled to first and second queues, the control circuit being operable to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is a Universal Serial Bus (USB) and the peripheral device is configured to transfer data over the bus using isochronous and bulk transfers.